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| THANGAVELU, KANDASAMY | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/273,560 | HASEGAWA, TAKUMI | |
| | Examiner | Art Unit | |
| | KANDASAMY THANGAVELU | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *October 8, 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Introduction*

1. This communication is in response to the Applicants' Amendment dated October 8, 2008. Claims 1-4 of the application were amended. Claims 1-6 of the application are pending. This office action is made final.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. §112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 5-6 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

3.1 Claim 5 states, "The delay analysis system as set forth in claim l, wherein the delay analyzing module determines automatically, based on the logical operation information of the logical circuit, that there is no change in a signal state of an output terminal of the logical circuit, and when no change in the signal state is determined, the delay analyzing module determines that no further delay analysis needs to be performed".

The Examiner checked carefully the entire specification and found that there is no support for "the delay analyzing module determines automatically, based on the logical operation information of the logical circuit, that there is no change in a signal state of an output terminal of the logical circuit, and when no change in the signal state is determined, the delay analyzing module determining that no further delay analysis needs to be performed" in the application. This is new material introduced in the amendment dated February 15, 2008 and is not allowed.

3.2 Claim 6 states, "The delay analysis system as set forth in claim 5, wherein the logical circuit is an AND gate, and when the logical operation information of the AND gate in the delay analysis library indicates that the state of the output terminal of the AND gate changes LOW-HIGH- LOW within a period of two clock signals, and at a time at which the second clock signal among the two clock signals is input, the state is LOW which is regarded to be the same state as the first signal state, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to a clock signal, the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate, and the delay analyzing module, based on the delay time information labeled as NONE, automatically determines that no further delay analysis needs to be performed in this case".

The Examiner checked carefully the entire specification and found that there is no support for "the delay analysis library not recognizing a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to a clock signal, the delay time information of the AND gate

being labeled as NONE indicating no change in the signal state at the output terminal of the AND gate, and the delay analyzing module, based on the delay time information labeled as NONE, automatically determining that no further delay analysis needs to be performed in this case" in the application This is new material introduced in the amendment dated February 15, 2008 and is not allowed.

***Claim Rejections - 35 USC § 101***

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claim 3 is rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter.

5.1 Claim 3 states, "A method of making delay analysis of a logical circuit, comprising:

referencing a delay analysis library for at least one circuit among a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information for said plurality of the circuits, …; and

automatically selecting a delay time of each path of said logical circuit from said delay time information, …".

Though the specification states that the method may be implemented in computer executable program, the claimed invention is broad enough to cover manual implementation of

the mathematical process of computing the delay time of each path from the information stored in a delay analysis library. Moreover, the process of "automatically selecting" is not described anywhere in the specification as including a computer implementation. A method that is not tied to other statutory class and does not convert physical matter or material into a different form is not statutory subject matter. Therefore this claim cannot be patented under 35 USC 101.

### *Claim Rejections - 35 USC § 103*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hasegawa** (U.S. Patent 6,041,168) in view of **Hasegawa** (U.S. Patent 5,528,511).

8.1 **Hasegawa** '168 teaches high-speed delay verification apparatus and method therefor. Specifically, as per Claim 1, **Hasegawa** '168 teaches a delay analysis system, executed on a computer, for making a delay analysis of a logic circuit (CL1, L5-8); the system comprising:

a delay analysis library comprising connection information and delay time information for a plurality of circuits (CL1, L58-61 and CL2, L30-35); and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library (Fig. 1, Item 7; CL4, L43-51; CL1, L58-61 and CL2, L30-35),

wherein, for at least one circuit of the plurality of circuits, the library further comprises logical operation information (CL1, L58-61 and CL2, L30-35),

wherein the delay analyzing module automatically analyzes the delay of the logical circuit based on the delay time information in the delay analysis library (Fig. 1, Item 7; CL4, L43-51; CL1, L58-61 and CL2, L30-35).

**Hasegawa** '168 does not expressly teach logical operation information comprising delay time information for a signal path from input terminals to output terminals of a logical circuit of the at least one circuit, wherein the delay time information is specific to an input terminal logical state transition of the logic circuit and resulting logical state transition at an output terminal of the logic circuit, and wherein the delay time information for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to the logical operation information. **Hasegawa** '511 teaches logical operation information comprising delay

time information for a signal path from input terminals to output terminals of a logical circuit of the at least one circuit, wherein the delay time information is specific to an input terminal logical state transition of the logic circuit and resulting logical state transition at an output terminal of the logic circuit, and wherein the delay time information for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to the logical operation information (Fig. 3; CL1, L28-35; CL2, L30-42; CL3, L5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; CL1, L28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; CL2, L30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; CL3, L5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Hasegawa** '168 with the system of **Hasegawa** '511 that included logical operation information comprising delay time information for a signal path from input terminals to output terminals of a logical circuit of the at least one circuit, wherein the delay time information is specific to an input terminal logical state transition of the logic circuit and resulting logical state transition at an output terminal of the logic circuit, and

wherein the delay time information for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to the logical operation information, because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process (CL2, L61-65).

8.2 As per Claim 2, **Hasegawa** '168 teaches a delay analysis system, executed on a computer, for making a delay analysis of a logic circuit (CL1, L5-8); the system comprising:

a delay analysis library comprising connection information and delay time information for a plurality of circuits (CL1, L58-61 and CL2, L30-35); and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library (Fig. 1, Item 7; CL4, L43-51; CL1, L58-61 and CL2, L30-35),

wherein, for each of the plurality of circuits, the library further comprises respective logical operation information (CL1, L58-61 and CL2, L30-35),

wherein the delay analyzing module automatically analyzes the delay of the respective logical circuit of each of the plurality of circuits based on the respective delay time information in the delay analysis library (Fig. 1, Item 7; CL4, L43-51; CL1, L58-61 and CL2, L30-35).

**Hasegawa** '168 does not expressly teach respective logical operation information comprising respective delay time information for a signal path from input terminals to output terminals of a respective logical circuit of each of the plurality of circuits, wherein the respective delay time information is specific to an input terminal logical state transition and resulting logical

state transition at an output terminal for the respective logical circuit of each of the plurality of circuits, and wherein the delay time information for each signal path of the plurality of circuits is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to the respective logical operation information for each of the plurality of circuits. **Hasegawa** '511 teaches respective logical operation information comprising respective delay time information for a signal path from input terminals to output terminals of a respective logical circuit of each of the plurality of circuits, wherein the respective delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for the respective logical circuit of each of the plurality of circuits, and wherein the delay time information for each signal path of the plurality of circuits is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to the respective logical operation information for each of the plurality of circuits (Fig. 3; CL1, L28-35; CL2, L30-42; CL3, L5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; CL1, L28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; CL2, L30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; CL3, L5-26 describes that the delay time information is stored for each rise/fall

type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

8.3 As per Claim 3, **Hasegawa** '168 teaches a method of making delay analysis of a logical circuit (CL1, L5-8); comprising:

referencing a delay analysis library for at least one circuit among a plurality of circuits, the delay analysis library comprising connection information, delay time information and logic operation information for the plurality of the circuits (CL1, L58-61 and CL2, L30-35).

**Hasegawa** '168 does not expressly teach that the delay time information comprises, for a logical circuit included in the at least one circuit, delay time information for a signal path from input terminals to output terminals of the logical circuit, and wherein the delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal of the logical circuit, the delay time information for each signal path of the logical circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at each output terminal as represented by the logical operation information for the at least one circuit. **Hasegawa** '511 teaches that the delay time information comprises, for a logical circuit included in the at least one circuit, delay time information for a signal path from input terminals to output terminals of the logical circuit, and wherein the delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal of the logical circuit, the delay time information for each signal path of the logical circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at each output terminal as represented by the logical

operation information for the at least one circuit (Fig. 3; CL1, L28-35; CL2, L30-42; CL3, L5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; CL1, L28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; C2, L30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; C3, L5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

**Hasegawa** '168 does not expressly teach automatically selecting a delay time of each path of the logical circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on an input terminal whose logical transition triggers the low state to the high state transition at the selected output terminal according to the logical operation information, or if the selected output terminal transitions from a high state to a low state, the delay time is selected based on an input terminal whose logical transition triggers the high state to the low state transition at the selected output terminal according to the logical operation information. **Hasegawa** '511 teaches automatically selecting a delay time of each path of the logical circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on an input terminal whose logical transition triggers the low state to the high state

transition at the selected output terminal according to the logical operation information, or if the selected output terminal transitions from a high state to a low state, the delay time is selected based on an input terminal whose logical transition triggers the high state to the low state transition at the selected output terminal according to the logical operation information (CL1, L28-35; CL2, L30-42; CL3, L5-26).

8.4 As per Claim 4, **Hasegawa** '168 teaches a computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer, perform a process for executing a delay analysis method for a logic circuit, the computer-readable medium causing a computer to execute the method (CL1, L5-8); wherein the method comprises:

referencing a delay analysis library for at least one circuit among a plurality of circuits, the delay analysis library comprising connection information, delay time information and logic operation information for the plurality of the circuits (CL1, L58-61 and CL2, L30-35).

**Hasegawa** '168 does not expressly teach that the delay time information comprises, for a logical circuit included in the at least one circuit, delay time information for a signal path from input terminals to output terminals of the logical circuit, and wherein the delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal of the logical circuit, the delay time information for each signal path of the logical circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at each output terminal as represented by the logical operation information for the at least one circuit. **Hasegawa** '511 teaches that the delay time information comprises, for a logical circuit included in the at least one circuit, delay time information for a

signal path from input terminals to output terminals of the logical circuit, and wherein the delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal of the logical circuit, the delay time information for each signal path of the logical circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at each output terminal as represented by the logical operation information for the at least one circuit (Fig. 3; CL1, L28-35; CL2, L30-42; CL3, L5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; CL1, L28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; C2, L30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; C3, L5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

**Hasegawa** '168 does not expressly teach automatically selecting a delay time of each path of the logical circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on an input terminal whose logical transition triggers the low state to the high state transition at the selected output terminal according to the logical operation information, or if the selected output terminal transitions from a high state to a low state, the delay time is selected based

on an input terminal whose logical transition triggers the high state to the low state transition at the selected output terminal according to the logical operation information. **Hasegawa** '511 teaches automatically selecting a delay time of each path of the logical circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on an input terminal whose logical transition triggers the low state to the high state transition at the selected output terminal according to the logical operation information, or if the selected output terminal transitions from a high state to a low state, the delay time is selected based on an input terminal whose logical transition triggers the high state to the low state transition at the selected output terminal according to the logical operation information (CL1, L28-35; CL2, L30-42; CL3, L5-26).

**Hasegawa** '168 does not expressly teach performing a delay calculation to determine a propagation delay time of the at least one circuit using the selected delay time of the logical circuit. **Hasegawa** '511 teaches performing a delay calculation to determine a propagation delay time of the at least one circuit using the selected delay time of the logical circuit (CL3, L5-26).

### *Response to Amendments*

9. Applicants' arguments, filed on October 8, 2008 have been considered. Applicant's arguments with respect to claim rejections under 35 USC 112 First paragraph are not persuasive. Claim rejections under 35 USC 101 are withdrawn for claims 1-2 and 5-6 in response to Applicant's arguments, but maintained for claim 3. Applicant's arguments with respect to claim rejections under 35 USC 103 (a) are not persuasive.

9.1 As per the applicants' argument that "at least Page 7, Line 22 to Page 8, Line 6 of the specification and Figs. 3-5 of the drawings support the features of claim 5; Fig. 3 is a waveform diagram showing the rise and fall delay patterns of a 2-input AND circuit; Fig. 3 is an example of the claimed delay time information in the delay analysis library; in the case where the input 1 rises and the input 2 falls, the specification discloses that no terminal is selected for delay analysis (specification, Page 8, Lines 5 and 6); that is, when no change in a signal state of an output terminal of the logic circuit is determined (Fig. 3, middle column – Rise/fall), the delay analysis module determines that no further delay analysis needs to be performed; this determination is necessarily automatic since it is based on the logical operation information of the logical circuit, which is stored in the delay analysis library ", the Examiner takes the position that Claim 5 does not have support in the specification, in spite of applicant's arguments.

The logical operation information does not have the capability to automatically determine based on the logical operation information of the circuit that there is no change in a signal state of an output terminal of the logical circuit. The applicant has not shown anywhere in the specification the existence of such capability. The applicant has not shown anywhere in the specification the support for "when no change in the signal state is determined, the delay analysis module determines that no further delay analysis is needs to be performed". Specification Page 7, Line 22 to Page 8, Line 6 and Figs. 3-5 do not support the above noted features. In Fig. 3, the showing of "NONE" when input 1 rises and input 2 falls is totally incorrect. How did the applicant select "NONE"? Ho can he justify such selection? In the AND circuit, the delay is

determined by the input rising later and the input falling earlier. Therefore, under Rise/Fall, the delay is determined first by input 1 that rises last and then by input 1 that falls earlier. This is what is done automatically. The use of "NONE" in Fig. 3 under Rise/Fall is incorrect. The applicant is arguing based on the incorrect table and has no basis for his argument.

9.2 As per the applicants' argument that "the portions of the specification and the drawings discussed with respect to claim 5 also support the features of claim 6; it appears that the Examiner's position is that since the claim features are not found explicitly in the specification, the subject claim limitation must not be supported by the disclosure; there is no word for word requirement for satisfying the written description requirement; in the exemplary embodiment of the claimed delay time information shown in Fig.3, it is shown in the middle column of the table in Fig. 3 (the rise/fall column) that the state of the output terminal of the AND gate changes LOW-HIGH-LOW within a period of two clock signals; it is shown that at a time at which the second clock signal among the two clock signals is input, the state is LOW which is same state as the first signal state; accordingly, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to the clock signal (see specification, Page 8, Lines 5 and 6); in this case the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate; therefore, the delay analysis module, based on this delay time information, automatically determines that no further delay analysis needs to be performed as recited in claim 6", the Examiner takes the position that Claim 6 does not have support in the specification, in spite of applicant's arguments.

The logical operation information does not have the capability to automatically determine based on the logical operation information of the circuit that there is no change in a signal state of an output terminal of the logical circuit. The applicant has not shown anywhere in the specification the existence of such capability. The applicant has not shown anywhere in the specification the support for "the delay analyzing module, based on the delay time information automatically determining that no further delay analysis is needs to be performed". Specification Page 7, Line 22 to Page 8, Line 6 and Figs. 3-5 do not support the above noted features. In Fig. 3, the showing of "NONE" when input 1 rises and input 2 falls is totally incorrect. How did the applicant select "NONE"? Ho can he justify such selection? In the AND circuit, the delay is determined by the input rising later and the input falling earlier. Therefore, under Rise/Fall, the delay is determined first by input 1 that rises last and then by input 1 that falls earlier. This is what is done automatically. The use of "NONE" in Fig. 3 under Rise/Fall is incorrect. The applicant is arguing based on the incorrect table and has no basis for his argument.

9.3 As per the applicants' arguments that the specification does provide support for computer implementation of the claimed method, the Examiner takes the position that claim 3 covers both computer implemented method and one that is not computer implemented. If claim 3 is limited to computer implemented method in which at least some of the steps are computer implemented, then it will be statutory.

9.4 As per the applicants' argument that "the invalidness specifier indicated by the invalidness specification in Fig. 7 of Hasegawa '511 is not, and cannot be automatically generated unlike the delay time information of claim 1; that is because in Hasegawa '511, the OR device of Fig. 2 is not always an OR device and moreover, there is no information provided in Hasegawa's delay analysis library of what logical circuit is the subject of the delay analysis; Hasegawa '511's Fig 3 is merely one example, which does not form the basis that the information of Fig. 7 is correct in all cases; manual judgment is necessary for preparing the information indicated by the invalidness specifier of Fig. 7; in the present invention, the delay analysis library already comprises logical operation information which in turn comprises delay information of the logical circuit, based on which the delay analysis module can automatically analyze the delay of the logical circuit; Hasegawa '511 alone or in combination with Hasegawa '168 does not teach or suggest this feature", the Examiner respectfully disagrees.

**Hasegawa** '511 shows at Fig. 3 the logical state transitions at each input terminal and logical state transitions at each output terminal. **Hasegawa** '511 discusses at CL1, L28-35 the logical state transitions at the input terminal and the output terminal, using rise/fall terms. **Hasegawa** '511 states at CL2, L30-42 that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid). The logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit. **Hasegawa** '511 describes at CL3, L5-26 that the delay time information is stored for each rise/fall type signal at various input and

output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified. Therefore, **Hasegawa** '511 teaches a method to automatically generate the delay time information of claim1; the **Hasegawa** '511 has the capability to indicate the circuit that is the subject of delay analysis (CL2, L61-65). Manual judgment is not necessary to prepare the information indicated by the invalidness specifier of Fig. 7, since the **Hasegawa** '168 library already contains logical operation information (CL1, L58-61 and CL2, L30-35).

### *Conclusion*

### *ACTION IS FINAL*

10. Applicant's arguments with respect to claim rejections under 35 USC § 103 (a) are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
January 17, 2009

/Paul L Rodriguez/
Supervisory Patent Examiner, Art Unit 2123